RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

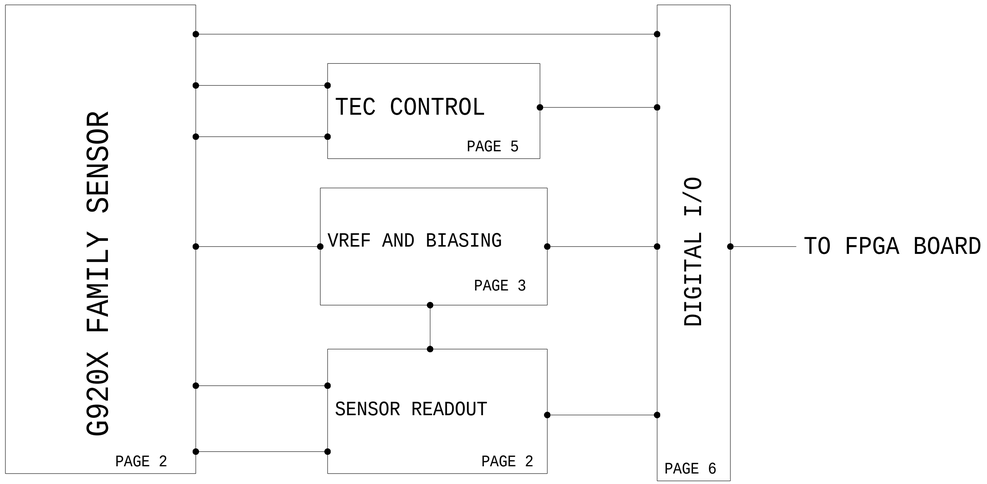
JUMPER TABLE

JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	29JAN18	S.HUNT



P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

TEMPLATE ENGINEER -	DATE	SCHEMATIC
HARDWARE SERVICES -		
HARDWARE SYSTEMS -		
TEST ENGINEER -		
COMPONENT ENGINEER -		
TEST PROCESS -		
HARDWARE RELEASE -		
DESIGNER R.ALAWAS	29JAN18	
PTD ENGINEER S.HUNT	29JAN18	
CHECKER -		

ANALOG DEVICES

HW TYPE : Customer Evaluation - Z
Product(s): ADN8835
: ADAQ7980
PACKAGE : N/A-lead N/A N/A-family
: Pitch-pitch StyleVendor Style

<User Define>
<User Define>
<User Define>

MASTER PROJECT TEMPLATE: TBD
TESTER TEMPLATE: no_template

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS X.XX +-0.010 X.XXX +-0.005
FRACTIONS +-1/32
ANGLES +-2

DRAWING NO. 02_048645
REV. B
SIZE D | SCALE 1:1 | CODE ID NO. CodeID | SHEET 1 OF 6

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

UA
UB
25-0513-10 TRUE
25-0513-10 TRUE

CENTER HOLE FOR A HEATSINK ON THE ARRAY
ARRAY IS SOCKETED
USE ARIES 25-0513-10 CUT TO 14-PIN STRIPS

G920X INGAAS ARRAY SENSOR
U2
DNI
RESET_EVEN
TE_POS
ADTRIG_EVEN
THERM_POS
THERM_NEG
CLK_EVEN
VIDEO_EVEN
CF_SELECT
RESET_ODD
TE_NEG
ADTRIG_ODD
VSS
INP
CLK_ODD
VREF
VREF_SENSOR
VIDEO_ODD
R57 20
R58 20
R65 499
SNS1 SNS2 SNS3 SNS4 SNS5 SNS6
DGND
AGND

L1
1KOHM AT 100MEGHZ
POS5VD
C8 0.1UF
C25 22UF
C4 0.1UF
C3 0.1UF
C38 270PF DNI
R4 TBD0603 DNI
R62 0
C29 27PF

ADA4807-1ARJZ
-IN
+IN
-VS
+VS
DISABLE_N
VOUT
U23
POS7VA
C9 0.1UF
C22 0.01UF

THIS CIRCUIT WAS DESIGNED FOR USE WITH THE FOLLOWING MODELS
G9201-256S
G9202-512S
G9203-256S
G9204-512S
WHICH ARE IN THE 28-PIN METAL PACKAGE AND HAVE 1-STAGE TE COOLING. IF USING A 2-STAGE TE-COOLED PART IN THE G92XX FAMILY, CHANGE THE VLIM AND ILIM OF THE TEC CONTROLLER ACCORDING TO THE DATASHEET, SCHEMATIC NOTES, AND UG-951.

VIDEO OUTPUT RANGE IS 0.76V TO 4.5V HERE.
ADD ADDITIONAL FILTERING HERE OR
AT THE OUTPUT OF BUFFER AMPLIFIERS

C37 270PF DNI
R63 0
R9 TBD0603 DNI
R64 499
C28 27PF
U14
ADA4807-1ARJZ
C83 0.1UF
C21 0.01UF

POS5VA
C17 0.1UF
U19
R1 499
R2 499 BAR_EVEN_ODD
ADG719BRMZ
R18 0
R17 TBD0603 DNI
C61 270PF DNI

NOTE: DEFAULT CONFIGURATION IS UNITY GAIN
REPLACE WITH *NOTED VALUES TO TRANSLATE
0V76 TO 4V56 TO FULL SCALE
OTHERWISE CALCULATE REQUIRED VALUES

POS5V_VREF
R5 100
C1 22UF
R7 2.74K 2K74*
R6 TBD0603 1K62*
R3 0 309R*
C41 270PF DNI
POS7VA
R8 0
C2 2.2UF
R10 10K
POS5VD
R59 0
C5 0.1UF
R98 10K
U1
ADAQ7980BCCZ
IN+ IN- AMP_OUT ADCN GND
REF_OUT REF GND V+ VDD PD_LDO_N LDO_OUT PD_REF_N PD_AMP_N V-
VIO SDI SCK SDO CNV
ADC_SDI ADC_SCLK SDO CONV
ADCVDD
R13 10K
R97 10K

C84 0.001UF
C85 0.001UF
C89 0.001UF
C95 0.001UF
AGND DGND

SNS7 SNS8 SNS9 SNS10 SNS11 SNS12 SNS13 SNS14 SNS15 SNS16
DGND AGND

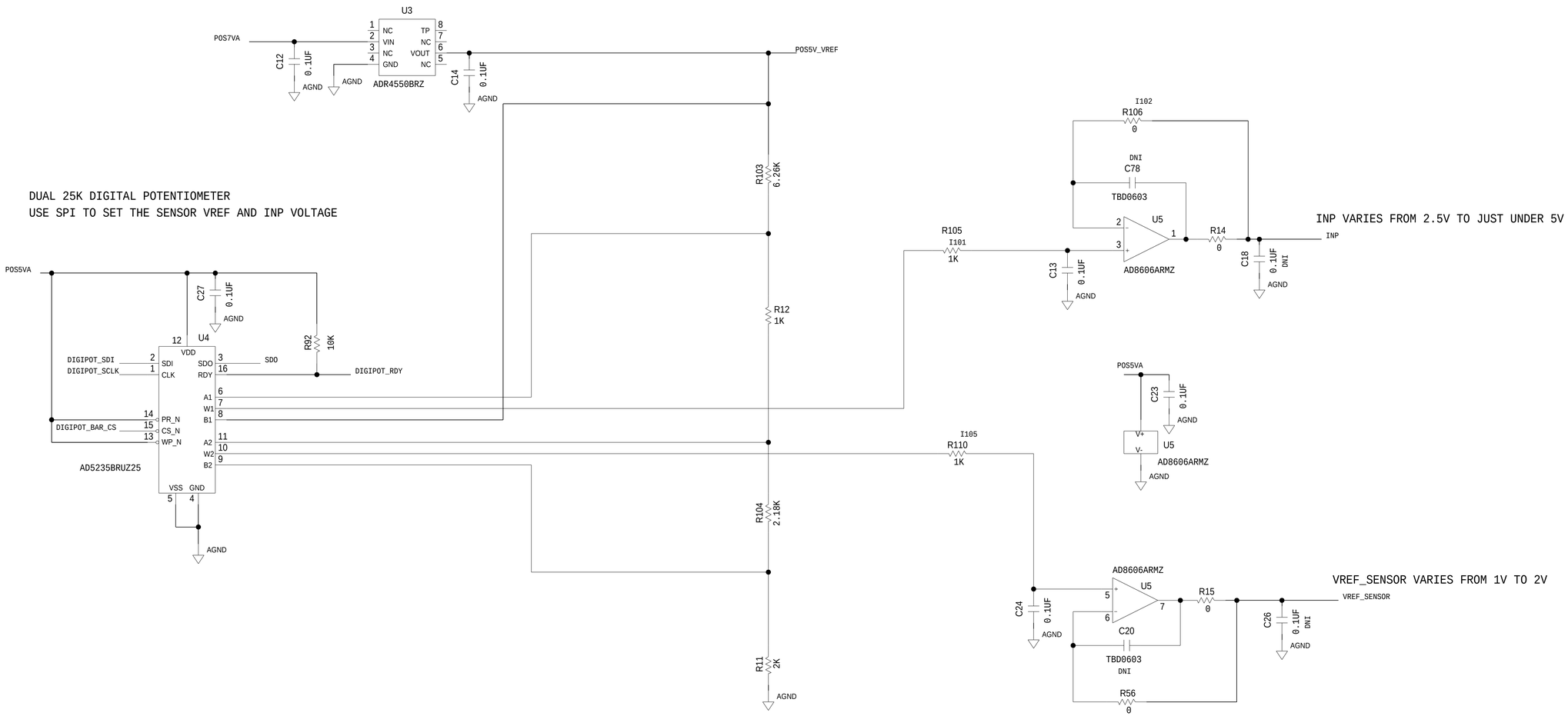
ANALOG DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation - Z
Product(s): ADN8835
: ADAQ7980

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_048645	B
PTD ENGINEER S.HUNT	SIZE D / SCALE 1:1	SHEET 2 OF 6

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ANALOG DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation - Z
Product(s): ADN8835
: ADAQ7980

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_048645	B

PTD ENGINEER	SIZE	SCALE	SHEET	OF
S.HUNT	D	1:1	3	6

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

USE 9VDC, 2 AMP ADAPTOR (500MA IS OKAY IF THERE IS NO TEC)
CENTRE POSITIVE

J2
PJ-002AH-SMT-TR
1A
1B
2
3
VIN
I193
F1
6A
I194
D1
SMAJ15CA-TR
I196
DGND
IRF9388TRPBF
Q5 I195
D
G
S
I197
R34
1K
I198
DGND
VIN_PROTECTED

POWER GOOD INDICATOR LEDS

POS5V_TEC
I209
SML-P11MTT86
DS3
I225
R20
100K
I210
R33
3K
I212
Q4
D
G
S
I213
PG5VTEC
R24
1K
2N7002T
I211
DGND

POS5VD
I204
SML-P11MTT86
DS1
I226
R19
100K
I205
R26
3K
I206
Q1
D
G
S
I207
PG5VA
R22
1K
2N7002T
I208
DGND

POS7VA
I201
SML-P11MTT86
DS2
I227
R21
100K
I203
R28
4.99K
I202
Q2
D
G
S
I199
PG7V
R23
1K
2N7002T
I200
DGND

I236
L2
0.47UH
I234
C30
4.7UF
I235
DGND
I237
P
N
C34
100UF
I238
DGND
C43
4.7UF
DGND
I222
R41
100K
BAR_TEC_SD
I223
R38
TBD0603
DNI
OPTIONAL: ALLOW FPGA CONTROL OF SHUTDOWN
BY TYING TO TEC CONTROLLER SHUTDOWN

LTM8053EY#PBF
I217
U8
VIN
VIN
VIN
VIN
RUN
SHARE
TR/SS
SYNC
RT
PG
TR_SS
SYNC_MODE
PG5VTEC
I220
R42
41.2K
1MHZ
I221
DGND
BIAS
AUX
VOUT
FB
GND
I218
R47
60.4K
5V
I219
DGND
POS5V_TEC
3.5A MAXIMUM
C39
100UF
C40
22UF
DGND

POS5V_TEC
I231
R39
TBD0603
I230
DNI
BAR_TEC_SD
R35
TBD0603
DNI
SYNC_MODE
I232
R40
TBD0603
DNI
I233
DGND

SYNC/MODE SELECTOR:
DEFAULT: FLOATING - PULSE-SKIP MODE
TIE TO GROUND FOR BURST MODE
USE VOLTAGE DIVIDER OF 2V9 TO 4V2 FOR SPREAD-SPECTRUM
TO SYNC WITH TEC CONTROLLER, CONNECT TO BAR_TEC_SD AND DRIVE WITH CLOCK

TR_SS
I228
C11
0.1UF
I229
DGND
SOFT START ~50MS

L8
1KOHM AT 100MEGHZ
C92
22UF
DGND
C6
0.1UF
DGND
U15
ADP7102ARDZ-5.0
PG5VA
VIN
PG
GND
EN_UVLO
VOUT
SENSE_ADJ
GND
NC
PAD
DGND
200MA MAXIMUM
C46
1UF
DGND
POS5VD
L11
1KOHM AT 100MEGHZ
C91
0.1UF
DGND
TO SENSOR
C47
22UF
DGND
C90
0.1UF
DGND
POS5VA

L9
1KOHM AT 100MEGHZ
C93
22UF
DGND
C74
0.1UF
DGND
U7
ADP7102ARDZ
PG7V
VIN
PG
GND
EN_UVLO
VOUT
SENSE_ADJ
GND
NC
PAD
DGND
R36
118K
R37
24.9K
DGND
R52
24.9K
C73
0.1UF
C7
0.1UF
I239
C35
22UF
I240
DGND
DGND
TO ANALOG FRONT END
POS7VA

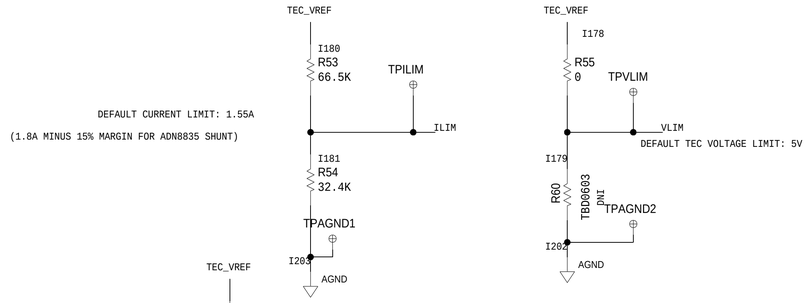
ANALOG DEVICES	SCHEMATIC	
	HW TYPE : Customer Evaluation - Z Product(s): ADN8835 : ADAQ7980	
THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_048645 / REV B
	PTD ENGINEER S.HUNT	SIZE D / SCALE 1:1 / SHEET 4 OF 6

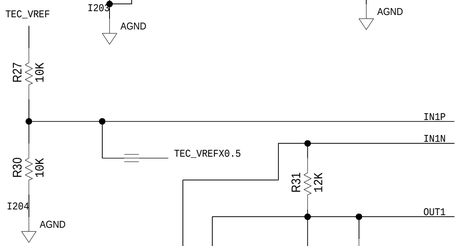
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

TEC CURRENT AND VOLTAGE LIMIT

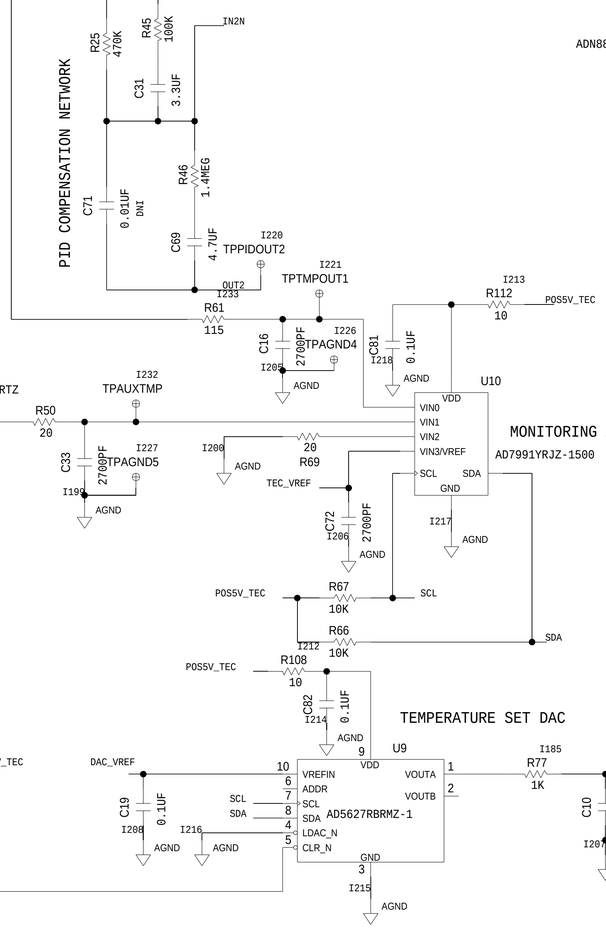
PLEASE CHECK THAT LIMITS ARE APPROPRIATE BEFORE USE.

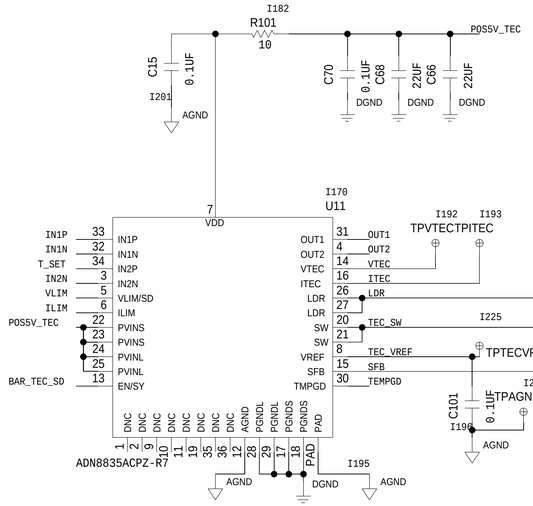
SEE ANALOG DEVICES UG-951 FOR RECOMMENDED
RESISTOR VALUES IF CHANGING MAX TEC CURRENT OR VOLTAGE

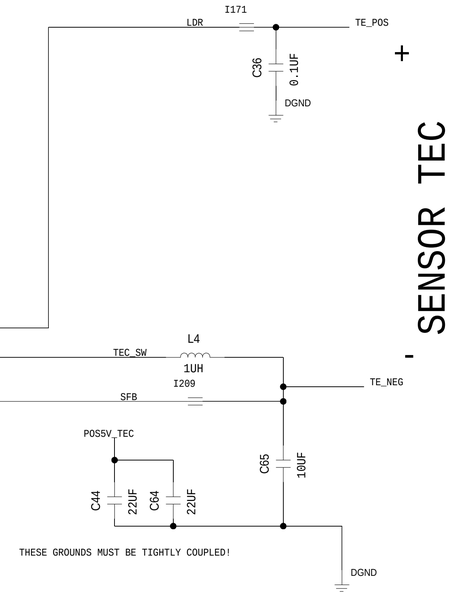




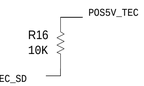
THERMISTOR CIRCUIT EXPECTS 5K OHM NOMINAL THERMISTOR WITH B = 3200
IF THIS IS NOT THE CASE, PLEASE RECALCULATE R32, R43, R31 VALUES





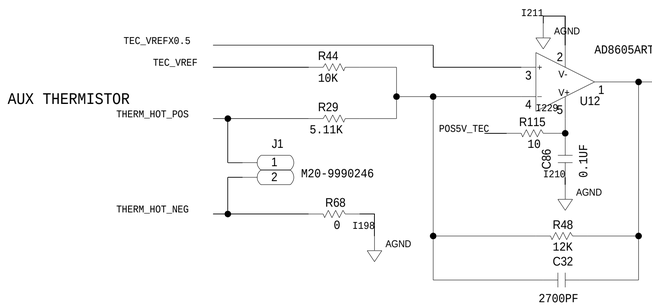


SHUTDOWN



BAR_TEC_SD CAN ALSO BE DRIVEN WITH A CLOCK BETWEEN 1.85 AND 3.25 MHZ TO SYNC. SEE DATASHEET.

AUX THERMISTOR



WITH R44=10K, R29=5.11K AND A THERMISTOR
OF 5K NOMINAL WITH B = 3200 AS IN THE TEC
THE OUTPUT OF U12 IS CENTERED AT VREFX0.5 AT 25C
AND CHANGES APPROXIMATELY +26.5MV/C

MONITORING ADC

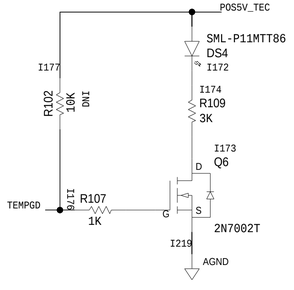
ABILITY TO SET THE TEMPERATURE PROGRAMMATICALLY IN THE TEC

ABILITY TO MEASURE THE TEMPERATURE WITH AN ADC

ABILITY TO MEASURE THE HOT TEMPERATURE WITH AN ADC (ANOTHER THERMISTOR)

ABILITY TO TURN OFF THE CHIP!

TEMP GOOD INDICATOR



TEMPERATURE SET DAC

WITH THERMISTOR COMPENSATION SHOWN IN THIS PAGE:

0 V SETS TEMP TP -29C

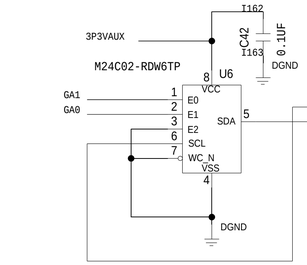
1.6 V SETS TEMP TO +40C

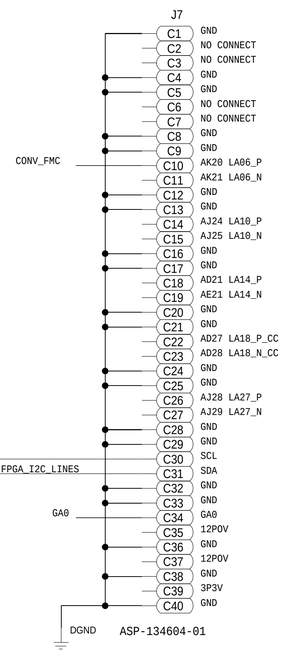
ANALOG DEVICES	SCHEMATIC		
	HW TYPE : Customer Evaluation - Z Product(s): ADN8835 : ADAQ7980		
THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_048645	REV B
	PTD ENGINEER S.HUNT	SIZE D	SCALE 1:1
		SHEET 5 OF 6	

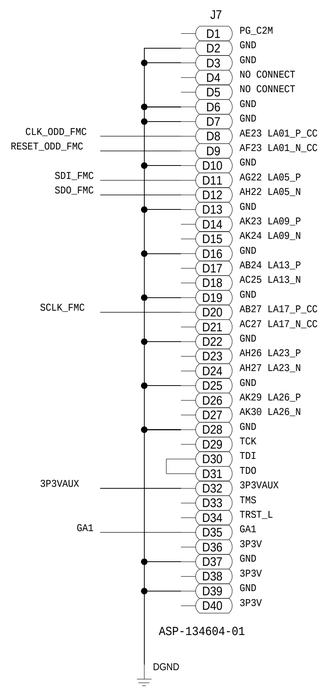
FMC-LPC CONNECTOR

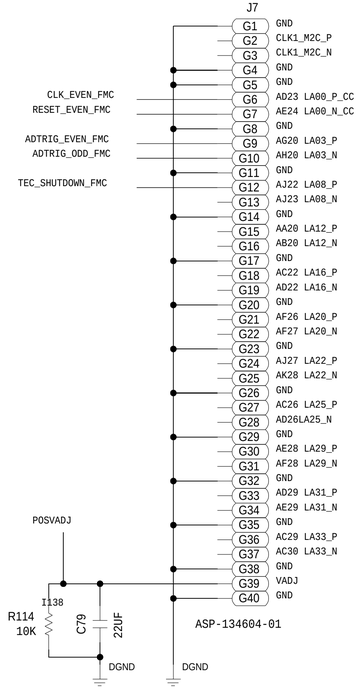
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

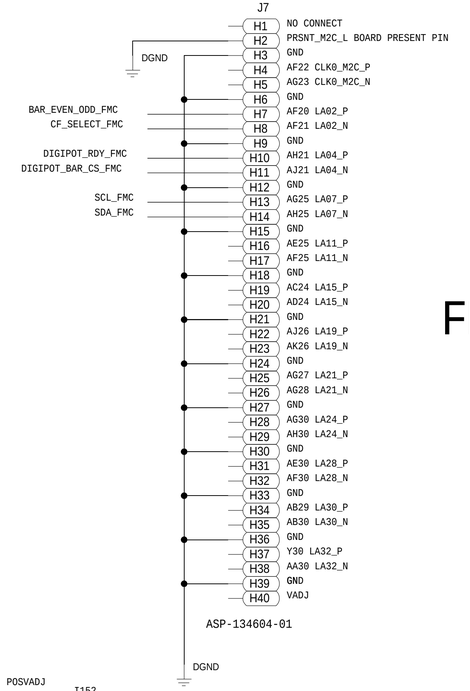
EEPROM REQUIRED IN VITA STANDARD
I2C LINE PULL-UP RESISTORS ON FPGA BOARD
I2C ADDRESS SET TO CONTROLLER BOARD



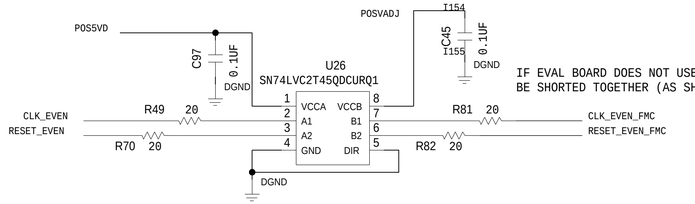


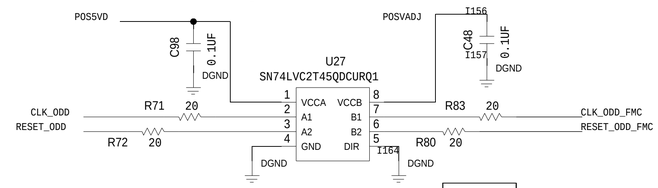


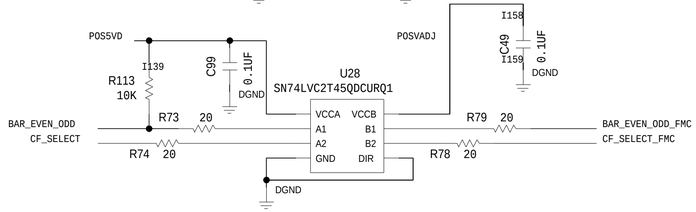


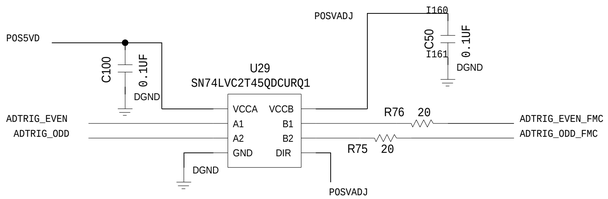


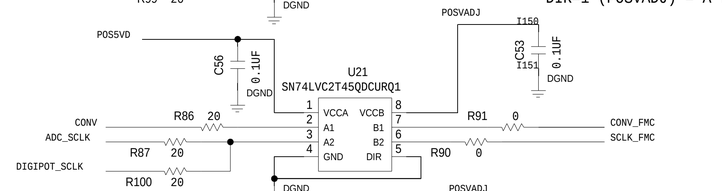
IF EVAL BOARD DOES NOT USE JTAG TDI AND TDO THEN THEY MUST
BE SHORTED TOGETHER (AS SHOWN) SO AS NOT TO BREAK JTAG CHAIN



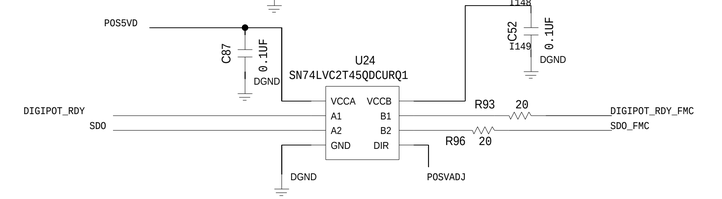


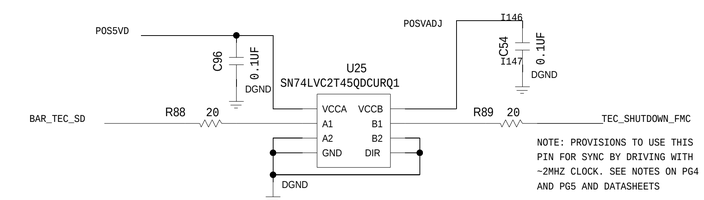


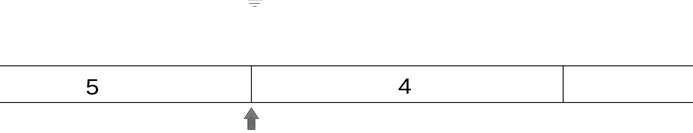




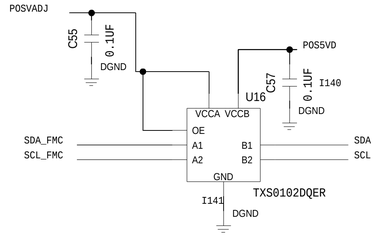
DIR=1 (POSVADJ) = A TO B







NOTE: PROVISIONS TO USE THIS PIN FOR SYNC BY DRIVING WITH ~2MHZ CLOCK. SEE NOTES ON PG4 AND PG5 AND DATASHEETS



ANALOG DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation - Z
Product(s): ADN8835
: ADAQ7980

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_048645	B
PTD ENGINEER: S.HUNT	SIZE: D / SCALE: 1:1	SHEET 6 OF 6